Sung Kim

Curriculum Vitae

University of Michigan
Ann Arbor, MI 48109
✉ *sungmk@umich.edu*
sungkim.net

Overview

My research is focused on hardware and algorithm design for high-performance and energy-efficient computer architectures, with an emphasis on accelerating emerging applications in machine learning and vision. I have also worked on new circuit-level building blocks for variation-tolerant SoCs, in particular for near-threshold and sub-threshold computing. My research and industry work incorporates experience from across the hardware/software stack, from systems software and application-level development, to architectural performance modeling and chip fabrication.

Education

University of Michigan — Ann Arbor, MI, USA
Ph.D., Electrical Engineering and Computer Science — 2018–pres.
- Advised by Hun-Seok Kim and Ron Dreslinski

University of Washington — Seattle, WA, USA
M.S., Electrical Engineering — 2015–2018
B.S., Electrical Engineering, Minor in Mathematics — 2011–2015
- Advised by Visvesh Sathe

Publications

Conferences

INFOCOM'18 **"Enabling Time-Critical Applications over Next-Generation 802.11 Networks"** (Demo Paper)
Sung Kim, Mohammad Mamunur Rashid, Saurabh Deo, Javier Perez-Ramirez, Mikhail Galeev, Ganesh Venkatesan, Sabyasachi Dey, William Li, Dave A. Cavalcanti
IEEE International Conference on Computer Communications, 2018
Best Demo Award

DATE'18 **"MATIC: Learning Around Errors for Efficient Low-Voltage Neural Network Accelerators"**
Sung Kim, Patrick Howe, Thierry Moreau, Armin Alaghi, Luis Ceze, and Visvesh Sathe
Design, Automation and Test in Europe, 2018
Best Paper Award

VLSI'18 **"An All-Digital Unified Clock Frequency and Switched-Capacitor Voltage Regulator for Variation Tolerance in a Sub-Threshold ARM Cortex M0 Processor"**
Fahim U. Rahman, **Sung Kim**, Naveen John, Roshan Kumar, Xi Li, Rajesh Pamula, Keith A. Bowman, and Visvesh Sathe
IEEE Symposium on VLSI Circuits, 2018

VLSI'18 **"An All-Digital True-Random-Number Generator with Integrated De-correlation and Bias Correction at 3.2-to-86 MB/s, 2.58 PJ/Bit in 65-nm CMOS"**
Rajesh Pamula, Xun Sun, **Sung Kim**, Fahim U. Rahman, Baosen Zhang, and Visvesh Sathe
IEEE Symposium on VLSI Circuits, 2018

ISSCC'18 **"A Combined All-Digital PLL-Buck Slack Regulation System with Autonomous CCM/DCM Transition Control and 82% Average Voltage Margin Reduction in a 0.6-1.0V Cortex-M0 Processor"**
Xun Sun, **Sung Kim**, Fahim U. Rahman, Rajesh Pamula, Xi Li, Naveen John, and Visvesh Sathe
IEEE International Solid State Circuits Conference, 2018

IISWC'17 **"Exploring Computation-Communication Tradeoffs in Camera Systems"**
Amrita Mazumdar, Thierry Moreau, **Sung Kim**, Meghan Cowan, Armin Alaghi, Luis Ceze, Mark Oskin, and Visvesh Sathe
IEEE International Symposium on Workload Characterization, 2017

ISC2'15 **"Motion-Vector Clustering for Traffic Speed Estimation from UAV Video"**
Ruimin Ke, **Sung Kim**, Zhibin Li, and Yinhai Wang
IEEE International Smart Cities Conference, 2015

E-Prints

arXiv'19 **"Bandwidth Extension on Raw Audio via Generative Adversarial Networks"**
Sung Kim, Visvesh Sathe
arxiv:1903.09027, 2019

Journals

JSSC'19 **"A Unified Clock and Switched-Capacitor-Based Power Delivery Architecture for Variation Tolerance in Low-Voltage SoC Domains"**
Fahim U. Rahman, **Sung Kim**, Naveen John, Roshan Kumar, Xi Li, Rajesh Pamula, Keith A. Bowman, Visvesh Sathe
IEEE Journal of Solid-State Circuits, 2019

JSSC'19 **"An All-Digital Fused PLL-Buck Architecture for 82% Average Vdd-Margin Reduction in a 0.6-to-1.0-V Cortex-M0 Processor"**
Xun Sun, Fahim U. Rahman, Rajesh Pamula, **Sung Kim**, Xi Li, Naveen John, and Visvesh Sathe
IEEE Journal of Solid State Circuits, 2019

SSCL'19 **"A 65nm CMOS 3.2-to-86 Mbps 2.58 pJ/b Highly Digital True-Random-Number Generator with Integrated De-correlation and Bias Correction"**
Rajesh Pamula, Xun Sun, **Sung Kim**, Fahim U. Rahman, Baosen Zhang and Visvesh Sathe
IEEE Solid-State Circuits Letters, 2019

TCAS-I'18 **"Energy-Efficient Neural Network Acceleration in the Presence of Bit-Level Memory Errors"**
Sung Kim, Patrick Howe, Thierry Moreau, Armin Alaghi, Luis Ceze, and Visvesh Sathe
IEEE Transactions on Circuits and Systems - I, 2018

ITS'16 **"Real-Time Bidirectional Traffic Flow Parameter Estimation from Aerial Videos"**
Ruimin Ke, Zhibin Li, **Sung Kim**, John Ash, and Yinhai Wang
IEEE Transactions on Intelligent Transportation Systems, 2016

Research and Industry Experience

University of Michigan — Ann Arbor, MI
Graduate Researcher — 2018–pres.
- Computer architecture and digital IC design; runtime-reconfigurable processors
- With Hun-Seok Kim and Ron Dreslinski

Intel Labs & Intel Programmable Solutions Group (Altera) — Hillsboro, OR
Research Intern — 2017–2018 (8 mo.)
- Hardware and systems development for wireless signal processing on SoC FPGAs
- With Mamun Rashid and Dave Cavalcanti

University of Washington — Seattle, WA
Graduate Researcher, Processing Systems Lab — 2015-2018
- Algorithm/hardware co-design for energy-efficient machine learning accelerators
- With Visvesh Sathe

NVIDIA Santa Clara, CA
Software Engineer Intern 2016 (5 mo.)
- EDA algorithm development, and applications of machine-learning for VLSI physical design
- With Vikas Agrawal and Ramesh Sundararaman

Electro Scientific Industries Portland, OR
Hardware Engineer Intern 2014 (4 mo.)
- Hardware development for industrial manufacturing lasers

University of Washington Seattle, WA
Undergraduate Researcher, M.P. Anantram Group and UW Photonics Lab 2013-2014
- Development of software tools for quantum device research, and optical trap experiments

InnovaTek Richland, WA
Engineering Intern 2011
- Hydrogen-reforming catalyst synthesis and characterization

Recognition

- INFOCOM Best Demo Award 2018
- DATE Best Paper Award 2018
- Tau Beta Pi and Eta Kappa Nu 2013
- Xerox Technical Scholarship 2012
- C.E. Boucher Scholarship 2011
- Dean's List 2011–2015

Teaching and Service

Reviewing
- *ACM International Conference on Mobile Computing and Networking (MobiCom)* 2020
- *IEEE Transactions on Circuits and Systems (TCAS)* 2019
- *IEEE International Symposium on Circuits and Systems (ISCAS)* 2019
- *Journal of Signal Processing Systems* 2018
- *IEEE Transactions on Intelligent Transportation Systems* 2017

Teaching Assistant, University of Washington.
- Design in Communications with Software-Defined Radio (EE 420) Spring 2018
- Digital VLSI Design I and II (EE 476/477) Winter 2015, Spring 2016
- Seattle MESA (volunteer tutor) 2015–2016

Mentorship
- Chi-Sheng Yang ECE M.S., 2019, University of Michigan
  CPU/GPU performance characterization on image and document analysis kernels
- Patrick Howe EE B.S., 2016, University of Washington
  FPGA verification and emulation of an OpenMSP430 microcontroller